REMARKS

This amendment is filed in response to the Patent Office Communication of September 20, 2006 advising Applicants that the amendment to Claim 19 filed July 28, 2006 introduced the limitation "third set of signal pads", which is a limitation of withdrawn Claim 10.

In a phone conference with Examiner Semenenko on September 28, 2006, it was clarified that Applicants' amendment filed July 28, 2006 was not entered, and the entire response to the rejection of May 2, 2006 should be resubmitted along with appropriate correction to the amendment of Claim 19 and any comments related thereto.

Applicants' previously presented amendment to claim 19 introducing the claim terminology "third set of signal pads" was undertaken in an effort to overcome the Examiner's rejection of Claims 19 - 21 under 35 USC 112, second paragraph.

Although it was not clear to Applicants why the Examiner considered Claim 19 indefinite, Applicants attempted, in their July 28, 2006 amendment, to further identify the limitation in the first para of Claim 19 calling for "respective signal pads positioned closer to the edge of said chip footprint". These are the signal pads 45, for example, in Fig. 7, which pads have vias connected thereto that extend to the next layer. The signal pads 45 are "positioned closer to the edge of said chip footprint" than the "second set of signal pads" 37 to which signal pads 45 are connected by a "conductive line" 38.

Thus, it appears to Applicants that the recitation in para 1 of Claim 19 calling for "a second set of signal pads (37) each having a conductive line (38) connected thereto

extending to connect to respective signal pads (45) positioned closer to the edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material" is clear and unambiguous. In this regard, the second set of signal pads 37 is a subset of all signal pads 37, some of which escaped (the first set of signal pads). The second set is clearly identified as those connected by conductive line 38 to pads 45.

In an effort to overcome the Examiner's objection to use of the term "third set of signal pads", Applicants now use the term "another set of signal pads". However, it should be noted that regardless of what term is used, it is clear that reference here is being made to essentially the same set of pads, i.e., structure, as identified in Claim 10 as a "third set of signal pads". Thus, Applicants see no substantive difference between the "third set of signal pads", as recited in Claim 10, and the "respective signal pads positioned closer to the edge of said chip" as originally recited in Claim 19 or, alternatively, the "another set of signal pads positioned closer to the edge of said chip", as proposed here in the amendment to Claim 19.

It is further noted that the claims in group I set forth in the restriction requirement of January 9, 2006 variously call for what amounts to "third set of signal pads" having "conductive vias connected thereto", as identified in Claims 10 - 18. For example, see the recitation "respective signal pads positioned nearer the said edge of said chip footprint" in Claim 1 and the recitation "wherein at least some of said signal pads on said dielectric layer nearer the said edge of said chip footprint have a conductive via connected thereto that form a set of conductive vias that extend through said layer of dielectric material", as recited in dependent Claim 2.

Thus, it appears to Applicants that the combination of layers and pads and vias exists in both Groups I and II. Applicants fail to see a subcombination in Group II or a structural difference between Groups I and II claims. The use in the preamble of the terms "multilayer chip carrier" in Group I and "multilayer chip carrier substrate" in Group II would not seem to be a valid basis for the restriction distinction since such terminology does not impart any difference into the structure that has been claimed in the body of the claims.

In summary to the Office Action of May 2, 2006, Claims 1 - 30 are pending in this application.

Claims 10 - 18 and 22 - 30 are withdrawn from consideration and Claims 1 - 9 and 19 - 21 have been rejected.

The Examiner has objected to the Drawings stating that "Figures 1 and 2 should be designated by a legend such as -- Prior Art --".

Accordingly, Applicants are submitting herewith new sheets 1 and 2 containing Figures 1 and 2, respectively. The new sheets identify Figures 1 and 2 as "Prior Art" and are labeled "Replacement Sheet". Applicants believe that the new sheets should overcome the Examiner's objection.

The Examiner has also objected to Claim 19 indicating that the recitation "the footprint" should be "a footprint". Accordingly, Claim 19 has been amended as indicated by the Examiner.

Claims 19 - 21 Rejection Under 35 USC112

Claims 19 - 21 have been rejected under 35 USC 112, second para, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

As stated earlier, it is not clear to Applicants what the Examiner finds indefinite. The Examiner states that it is assumed that "a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads of the first set of signal pads positioned closer to the edge of said chip footprint with the signal pads of the second set of signal pads having conductive vias connected thereto extending through said first layer of dielectric material" (emphasis added). This assumption is incorrect.

Applicants believe that Claim 19 clearly states the structure disclosed by Applicants and such structure so clearly stated is not that assumed by the Examiner.

Claim 19 recites "a second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned closer to the edge of said chip footprint with said signal pads positioned closer to the edge of said chip footprint having conductive vias connected thereto extending through said first layer of dielectric material". The "respective signal pads positioned closer to the edge of said chip footprint" are a new set of signal pads and not the "first set of signal pads", as assumed in the underlined portion of the above-quoted Examiner's statement.

Again, as stated earlier, the "second set of signal pads" reads on the set of signal pads 37 which did not escape (the first set of signal pads escaped) and is a subset of "a plurality of signal pads" formed on the first dielectric layer. The set of signal pads 37 which did not escape at this level are connected by lines 38 to signal pads 45 and this corresponds to the recitation "a second set of signal pads (pads 37 that did not escape) each having a conductive line (lines 38) connected thereto extending to connect to respective signal pads (pads 45) positioned closer to the edge of said chip footprint".

Thus, pads 45 act to move the signal lines closer to the edge of the chip footprint. These pads, i.e., pads 45, have "conductive vias connected thereto extending through said first layer of dielectric material".

Although Applicants believe that Claim 19 is clear, definite and particularly points out and distinctly claims the subject matter that Applicants regard as their invention, Applicants have amended Claim 19 to even more clearly set forth Applicants' invention. For example, as amended, the "respective signal pads" are now set forth as "respective signal pads of another set of signal pads". The "conductive vias" are now set forth as "a set of conductive vias in said first layer of dielectric material". The recitation in Claim 19, para 2, relating to the second layer of dielectric material similarly sets forth first and second sets of signal pads and a set of conductive vias. Applicants believe that Claim 19 is clear and unambiguous and, moreover, is clearly allowable over the art relied upon by the Examiner, as will be pointed out hereinafter.

Claims 1 - 4, 8, 9 and 19 - 21 Rejection Under 35 USC 103(a) on APA in views of Buschbom

Claims 1 - 4, 8, 9 and 19 - 21 have been rejected under 35 USC 103(a) as being obvious over APA in view of Buschbom (USP6800944). In this rejection, the Examiner asserts that independent Claim 1 reads on APA except APA does not explicitly teach that the "second set of signal pads each having a conductive line connected thereto extending to connect to respective signal pads positioned nearer the said edge of said chip footprint". The Examiner goes on to state, however, that "Buschbom discloses in prior art drawing of Fig. 2 set of said signal pads 14, 46 (Column 3, lines 62 - 67) each having a conductive line 15, 44 connected thereto extending to connect to respective signal pads 14 positioned nearer the said edge of said chip footprint". From this, the Examiner concludes that it would be obvious to construct in the APA "a second set of signal pads each having a conductive line connected thereto extending to respective signal pads positioned nearer the said edge of said chip footprint".

It appears that, in this rejection, the Examiner is conveniently lifting structure from Buschbom and positioning it in the APA in an effort to construct a device to anticipate Applicants' claimed invention and, in doing so, is using Applicants' teachings.

The Buschbom invention is completely devoid of any teaching in regard to a multilayer microvia chip carrier 3 "wireability", i.e. the technical possibility of positioning routing lines so that all signals may "escape" from a given pattern (see Applicants' page 2). Buschbom is concerned with the problem of prior art substrates

wherein each contact terminal and trace is required to be electrically coupled to a plating bus at the score line in order to electroplate the contact terminals and traces (See Col. 4, lines 30 et seq. of Buschbom). The Buschbom patent is directed to solving this problem. Incidental to this, Buschbom shows one pad connected by a line trace to another pad in the context of showing how connection to the plating bus is problematic.

Accordingly, there is nothing in Bushbom to suggest that the Buschbom structure could be combined with the APA. Buschbom is directed to a single layer chip carrier and proposes the use of electroless plating to eliminate plating stubs and allow formation of a ground ring around the pattern of contact pads. There is nothing in Buschbom to teach or suggest that the Buschbom structure in question could be used to improve wireability and increase available chip carrier real estate.

Insofar as Applicants are aware, prior art escape patterns and procedures do not take advantage of moving signal pads that do not escape at one escape level closer to the edge of the chip footprint at that level so as to facilitate escape at subsequent levels. Applicants do this by using unused space nearer the chip footprint edge. Applicants, in fact, disclose using this technique at least twice such that the cumulative advantage is the creation of more space for power PTHs, for example, at a subsequent level.

No Prima Facia Case of Obviousness

Applicants do not believe that the Examiner has established a prina facia case of obviousness in combining Buschbom with APA. As is known, to establish a prima facia case of obviousness three criteria must be met. First, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or combine references teachings. Second, there must be some reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. In this regard, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon Applicants' disclosure.

Applicants believe that the Examiner's rejection of Claims 1 - 4, 8, 9 and 19 - 21 under 35 USC103(a) on APA and Buschbom fails to meet these criteria. In this regard, the rejection of Claim 19 on APA and Buschbom not only clearly fails to meet the first criteria, but also clearly fails to meet the second and third criteria.

In rejecting independent Claim 19, the Examiner again erroneously relies upon Buschbom in constructing structure on the first layer of dielectric material, as done in the rejection of independent Claim 1. However, in addition to this, it appears the Examiner has overlooked claim limitations in regard to the recited "second layer of dielectric material". For example, the APA (FC 2 layer) does not show "respective conductive lines connected thereto extending to respectively connect to further signal pads closer to the edge of said chip footprint" (emphasis added). This recitation is akin to the recitation in regard to the "first layer of dielectric material" and acts to further move the signal pads closer to the edge of the chip footprint to thereby free up space for the next level.

In rejecting Claim 19, the Examiner also asserts that, in regard to the recited third layer, that a duplication of parts is involved. In this regard, the Examiner relies upon In re Harza, 274 F2d 669, 124USPQ378 (CCPA 1960). Applicants are not clear from the Examiner's statements, how this decision applies to the recited "third layer of dielectric"

claim limitations. However, it is to be noted that although Applicants' invention is directed to a multilayer chip carrier, that does not mean the layers are duplicates. Each layer has its own function and what Applicants have done is routed the wiring on the respective levels so as to ultimately free up space at the FCI signal redistribution level to make more room for power PTH's, for example. In this regard, it should be noted that chip carrier real estate, i.e., available usable space in chip carriers, is very expensive and making efficient use of such space is a very important objective is the electronic industry.

It should be noted that Claims 1 - 4, 8 and 9 include limitations akin to those recited in Claim 19 in regard to the first and second layer of dielectric material. Accordingly, rejection of these claims on APA and Bushbom fails for the same reasons given in regard to the rejection of Claim 19 and the Claim 19 limitations.

Claims 5 - 7 Rejection Under 35 USC103(a) on APA in view of Buschbom in further View of Arimi

It is not clear to Applicants how Arimi applies to Claim 5 - 7. Claim 5, for example, recites limitations that call for vias extending through the second ("further") layer of dielectric material to pads on a third ("another") layer of dielectric material, the latter pads of which have conductive lines that "escape". Thus, Claim 5 is akin Claim 19 in regard to the limitations recited with reference to the first, second and third layers of dielectric material, and it is to be noted that Claim 19 was rejected without Arima. It is not clear what Arima adds to the rejection. Moreover, Arima is directed to a wiring board layout of signal wiring and power supply wiring terminals that reduces crosstalk. There is

nothing in Arima to suggest that it could be combined in some manner with APA and Buschbom.

Conclusion

In view of Applicants' amendment and remarks, Applicants firmly believe that the application is now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejections, and allow the claims as now presented and pass the case to issue.

Respectfully submitted,

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